AMENDMENTS TO THE SPECIFICATION

Page 2, 3rd full paragraph:

In the above-described second prior art GaAs heterojunction field effect type semiconductor device, since the carbon-doped p^+-type GaAs layer forms a p^+-n junction with its ~~underlaying~~ underlying layers, an effective Schottky barrier against electrons within a channel formed in the undoped InGaAs channel layer is substantially increased. That is, this effective ~~Schottoky~~ Schottky barrier is increased to a degree of the bandgap of the carbon-doped p^+-type GaAs layer such as 1.4eV.

Page 3, 1st full paragraph:

In a third prior art GaAs heterojunction field effect type semiconductor device (see: K. NISHI et al., "High Current/gm self-Alignment PJ-HFET of Completely Enhancement-Mode Operation", Extended Abstracts of the 1998 International Conference on Solid-State Devices and Materials, pp. 396-397, 1998), a channel layer, an undoped AlGaAs Schottky layer, an undoped GaAs Schottky layer and a carbon-doped p^+-type GaAs layer are sequentially grown at an epitaxial growth process. Also, a gate electrode is formed on the carbon-doped p^+-type GaAs layer. Further, ~~n^+-type contact regions, and~~ an ohmic source electrode and an ohmic drain electrode are formed on the n^+-type contact regions. This also will be explained later in detail.

Page 4, 1st full paragraph:

It is an object of the present invention to provide a heterojunction field effect type semiconductor device having a high gate turn-on voltage and a low ON-resistance.

Pages 6-7, bridging paragraph:

In Fig. 1, which illustrates a first prior art GaAs heterojunction field effect type semiconductor device (see: Yasunori BITO et al., Fig. 2 of "64% Efficiency Enhancement-Mode power Heterojunction FET for 3.5V Li-Ion ~~Baffery~~ Battery Operated Personal Digital Cellular Phones", 1998 IEEE MTT-S Int. Microwave Symp-Dig., pp. 439-442, June 1998), reference numeral 1 designates a semi-insulating GaAs substrate. Also, an undoped AlGaAs buffer layer 2, an Si-doped n^+-type AlGaAs electron supply layer 3, an undoped AlGaAs spacer layer 4, an undoped InGaAs channel layer 5, an undoped AlGaAs spacer layer 6, a Si-doped n^+-type AlGaAs electron supply layer 7, an undoped AlGaAs Schottky layer 8, an undoped GaAs Schottky layer 9, a Si-doped n^+-type AlGaAs wide recess etching stopper layer 10 and a Si-doped n^+-type GaAs cap layer 11 are sequentially grown on the GaAs substrate 1 by an epitaxial growth process. Also, an insulating layer 12 made of silicon dioxide is formed on the undoped GaAs Schottky layer 9. Further, a gate electrode 13 made of aluminum or the like is formed on the undoped AlGaAs Schottky layer 8 via a recess within the undoped GaAs layer 9. Additionally, an ohmic source electrode 14S and an ohmic drain electrode 14D made of AuGe/Au or the like are formed on the Si-doped n^+-type GaAs cap layer 11.

Pages 7-8, bridging paragraph:

In Fig. 2, which illustrates a second prior art GaAs heterojunction field effect type semiconductor device (see: Shigeki WADA et al., "0.1-μm p^+-GaAs Gate HJFET's Fabricated Using Two-Step Dry-Etching and Selective MOMBE Growth Techniques", IEEE Transactions on Electron Devices, Vol. 45, No. 6, pp. 1383-1389, June 1998), reference numeral 201 designates a semi-insulating GaAs substrate. Also, an undoped AlGaAs buffer layer 202, an Si-doped ~~n-type~~ n^+-type AlGaAs electron supply layer 203, an undoped InGaAs channel layer 204, a Si-doped ~~n-type~~ n^+-type AlGaAs electron supply layer 205, an undoped AlGaAs Schottky layer 206, and a Si-doped n^+-type GaAs cap layer 207 are sequentially grown on the GaAs substrate 201 by a first epitaxial growth process. Also, an insulating layer 208 made of silicon dioxide is formed on the undoped AlGaAs Schottky layer 206. Further, a carbon-doped p^+-type GaAs layer 209 is grown on the undoped AlGaAs Schottky layer 206 via a recess within the insulating layer 208 by a second epitaxial growth process. Additionally, a gate electrode 210 made of aluminum or the like is formed on the carbon-doped p^+-type GaAs layer 209. Further, an ohmic source electrode 211S and an ohmic drain electrode 211D made of AuGe/Au or the like are formed on the Si-doped n^+-type GaAs cap layer 207.

Page 8, 1st full paragraph:

In the GaAs heterojunction field effect type semiconductor device of Fig. 2, since the carbon-doped p^+-type GaAs layer 209 forms a p^+-n junction with its ~~underlaying~~ underlying layers, an effective Schottky barrier against electrons within a channel formed in the undoped

InGaAs channel layer 204 is substantially increased. That is, this effective ~~Schottoky~~ Schottky barrier is increased to a degree of the bandgap of the carbon-doped p^+-type GaAs layer 209 such as 1.4eV.

Pages 8-9, bridging paragraph:

The reason why the gate turn-on voltage V_f is not so increased is that the carbon-doped p^+-type GaAs layer 209 is epitaxially grown directly on the undoped AlGaAs Schottky layer 206. That is, since the undoped AlGaAs Schottky layer 206 is exposed to the air, the aluminum component of the undoped AlGaAs Schottky layer 206 actively reacts with oxygen so that aluminum oxide is created thereon. Since the aluminum oxide is difficult to be removed, the aluminum oxide induces defects in the epitaxially-grown carbon-doped p^+-type GaAs layer 209, so that the gate turn-on voltage V_f is decreased to create a gate leakage current.

Pages 21-22, bridging paragraph:

Further, in the above-described embodiments, the insulating layer [[13]] 12 can be made of SiN_x or SiN_xO.